STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

1. **(Original)** An integrated circuit, comprising:
   (a) a clock divider circuit comprising:
      (i) a counter operatively configured to generate a plurality of first signals from a second signal, each one of said plurality of first signals having a first phase and said second signal having a second phase; and
      (ii) a mux in electrical communication with said counter and operatively configured to output a selected one of said plurality of first signals; and
   (b) a phase detector operatively configured to detect an offset between said first phase of said selected one of said plurality of first signals and said second phase of said second signal and generate a third signal representing said offset.

2. **(Original)** An integrated circuit according to claim 1, further comprising a clock mesh having a mesh delay and delay circuitry, wherein said selected one of said plurality of first signals propagates to said phase detector through said clock mesh and said delay circuitry is operatively configured to simulate said mesh delay, said second signal propagating to said phase detector through said delay circuitry.

3. **(Original)** An integrated circuit according to claim 1, wherein said selected one of said plurality of first signals has a frequency equal to the frequency of said second signal divided by an even integer n and said phase detector is operatively configured to measure said selected one of said plurality of first signals n/2 times to determine said offset.

4. **(Original)** An integrated circuit according to claim 1, wherein said counter comprises a plurality of latches each corresponding to a corresponding one of said plurality of first signals, the integrated circuit further comprising counter reset circuitry responsive to said third signal so as to reset to zero the one of said plurality of latches corresponding to said selected one of said plurality of first signals and each one of said plurality of latches that is of a lower order than the one of said plurality of latches corresponding to said selected one of said plurality of first signals.

5. **(Original)** An integrated circuit according to claim 4, wherein said third signal represents a binary offset and said counter reset circuitry subtracts said binary offset from said counter.

6. **(Original)** A system, comprising:
   (a) a plurality of processors each comprising:
      (i) a clock divider circuit that includes:
         (1) a counter operatively configured to generate a plurality of first signals from a second signal, each one of said plurality of first signals having a first phase and said second signal having a second phase; and
         (2) a mux in electrical communication with said counter and operatively configured to output a selected one of said plurality of first signals; and
      (ii) a phase detector operatively configured to detect an offset between said first phase of said selected one of said plurality of first signals and said second phase of said second signal and generate a third signal representing said offset; and
   (b) a synchronization initiation circuit in electrical communication with said phase detector of each of said plurality of processors and operatively configured to provide a synchronization signal to each of said phase detectors for initiating detection of each said offsets.

7. **(Original)** An integrated circuit according to claim 6, wherein at least one of said selected ones propagates to the corresponding one of said phase detectors through a clock mesh having a mesh delay, the corresponding one of said plurality of processors further comprising delay circuitry operatively configured to simulate said mesh delay, said second signal of the corresponding one of said plurality of processors propagating to the corresponding one of said phase detectors through said delay circuitry.

8. **(Original)** An integrated circuit according to claim 6, wherein each one of said selected ones has a frequency equal to the frequency of the corresponding one of said second signal divided by an even integer n and the corresponding one of said phase detector is operatively configured to measure the corresponding one of said selected ones n/2 times to determine the corresponding one of said offsets.

9. **(Original)** An integrated circuit according to claim 6, wherein each one of said counters comprises a plurality of latches each corresponding to a corresponding one of said plurality of first signals, each one of said plurality of processors further comprising counter reset circuitry responsive to the corresponding one of said third signals so as to reset to zero the one of said plurality of latches corresponding to said selected one of said plurality of first signals and each one of said plurality of latches that is of a lower order than the one of said plurality of latches corresponding to said selected one of said plurality of first signals.

10. **(Original)** An integrated circuit according to claim 9, wherein each one of said third signals represents a binary offset and the corresponding one of said counter reset circuitry subtracts said binary offset from the corresponding one of said counter.

11. **(Original)** A method of resetting at least one divide-by counter having an input signal with a first phase, the divide-by counter outputting a plurality of divide-by signals each having a second phase, the method comprising the steps of:
    (a) selecting one of the plurality of divide-by signals;
    (b) determining a phase offset between the second phase of said selected one of the plurality of divide-by signals and the first phase of the input signal; and
    (c) resetting the divide-by counter based upon said phase offset.

12. **(Original)** A method according to claim 11, wherein said selected one of said plurality of divide-by signals propagates through a clock mesh that causes a mesh delay, the method further comprising a step of simulating said mesh delay in the input signal.

13. **(Original)** A method according to claim 11, wherein step (b) includes measuring the magnitude of said selected one of the plurality of divide-by signals.

14. **(Original)** A method according to claim 13, wherein the input signal has a plurality of edges and a plurality of cycles, the method further comprising prior to step (b) the step of providing a synchronization pulse so as to identify which one of the plurality of edges of input signal to use in step (b) as a reference edge, the step of measuring the magnitude of said selected one of the plurality of divide-by signals including measuring the magnitude of said selected one

of the plurality of divide-by signals in ones of the plurality of cycles immediately following said reference edge.

15. **(Original)** A method according to claim 14, wherein the input signal has a first frequency and said selected one of the plurality of divide-by signals has a second frequency equal to $1/(2^n)$ times the first frequency, wherein n is an integer, the step of measuring the magnitude of said selected one of the plurality of divide-by signals including taking a measurement during each of $(2^n)/2$ cycles of the input signal.

16. **(Original)** A method according to claim 11, wherein each one of a plurality of divide-by counters are synchronized by performing steps (b) and (c) substantially simultaneously with one another.

17. **(Original)** A method according to claim 16, further including prior to step (b) the step of providing a synchronization pulse so as to initiate step (b) relative to each one of the plurality of divide-by counters.

18. **(Original)** A method according to claim 11, wherein said offset signal represents a binary offset and step (c) comprises subtracting said binary from the at least one divide-by counter.

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